

In maintaining the Examiner's outstanding 35 USC §103 obviousness rejection, the Examiner now relies on new references (namely, Fujimoto, U.S. Patent No. 5,115,545, and DiStefano, U.S. Patent No. 5,548,091) in rejecting claims 1 - 8 under 35 USC §103 based on the applicants' discussion of the prior art¹ in view of Maeda (U.S. Patent No. 4,880,486), Fujimoto and DiStefano.

As to the first two cited references, such references have been discussed in the last Amendment filed for this case. Also, with respect to such first two cited references, the Examiner has acknowledged that:

the combination of applicant[s'] admitted prior art and Maeda teaches a process comprising plural chips, the combination does not explicitly teach a process wherein a second fixing is simultaneously performed for each of the chips with a second pressure.²

However, in supplementing such acknowledged deficiencies or drawbacks in the teachings of the first two cited prior art, the Examiner argues that the teachings of Fujimoto supplement the above-discussed deficiencies or drawbacks in the teachings of the first two cited references, and specifically relies on Fujimoto's lines 58 - 63, column 5.

¹ That is, line 23, page 1 through line 22, page 2 of the applicants' specification, and as illustrated in the applicants' Figures 1A through 1E.

² See, lines 1 - 5, page 4 of the outstanding Action.

In addition, in the paragraph bridging page 4 and 5 of the outstanding Action, the Examiner has acknowledged that:

although the combination of applied prior art teaches a process comprising the steps of heating with a half-thermosetting temperature, aligning and first fixing the chips, the applied prior art does not explicitly teach a process comprising **concurrently** heating with a half-thermosetting temperature, aligning and first fixing the chips.³

Emphasis in original. However, in supplementing such deficiencies or drawbacks in the teachings of the cited references, the Examiner specifically relies on line 3, column 9 through line 2, column 10 in DiStefano.

First, as pointed out to the Examiner during a personal interview conducted on May 20, 1997 to which the applicants respectfully acknowledge with appreciation, the following are two conditions required when fixing a bare chip to a circuit board or the like: (1) there must be viscosity for preventing a positioned chip from moving in order to have such chip provisionally fixed to such circuit board; and (2) there must be liquidity for allowing the adhesive to be pushed out to a periphery of such chip when positioning the chip and pushing such chip against the circuit board.

Secondly, significant structural features of the applicants' claimed fabrication method include the steps of: (1) heating of the adhesive on the substrate at a half-thermosetting temperature; and (2) simultaneous with such heating step, aligning the chips to the mounting

³ See, the paragraph bridging pages 4 and 5 of the outstanding Action.

parts of the substrate. As such, even if the adhesive has been substantially hardened by a fast thermosetting process, the chip has been previously aligned and fixed by the first fixing pressure. Thus, it is not necessary in the applicants' claimed invention to precisely adjust viscosity of the adhesive.

Thirdly, with respect to the required liquidity, in the applicants' claimed invention, there is a large number of chips to be fixed; thereby, requiring liquidity for the adhesive to pass through or be pushed out to the peripheries of the chips having small intervals therebetween. In the secondary reference of, for example, Fujimoto, there are small numbers of terminals having large intervals therebetween; as such, if Fujimoto's process is used in the claimed invention, there would be insufficient liquidity for the adhesive to pass through very short intervals between the large number of chips or terminals.

Additionally, it is the applicants' understanding the Examiner noted that, contrary to what was said in the outstanding Action⁴, the secondary reference of DiStefano is merely relied upon for teaching simultaneous or concurrent heating and aligning of chips, and not for the teaching of half-thermosetting. Also, Fujimoto is not relied upon for teaching a step of heating at a half-thermosetting temperature.

Moreover, it is the Maeda reference which, according to the Examiner, teaches the step of heating at a half-thermosetting temperature, and does not teach the simultaneous or

⁴ See, the paragraph bridging pages 4 and 5 of the outstanding Action.

concurrent heating and aligning of chips.

Furthermore, line 57, column 3 through line 55, column 4 in Maeda set forth in pertinent parts the following:

The printed circuit substrate 1 bearing such a pressure-sensitive adhesive is set on an automatic parts-loading machine, and the chip-type electronic parts 4 are loaded one-by-one on selected positions where the adhesive is already gelated, and adequately pressed by a mounting head for adhering the electronic parts on the substrate as shown in FIG. 2(b).

* * *

Thereafter, ultraviolet rays are irradiated for ten seconds on the adhesive 3 for gelating the adhesive so as to destroy the fluidity thereof and to give pressure-sensitive adhesion ability thereto by using a high-pressure mercury lamp in which the infrared rays are reduced by mercury lamp in which the infrared rays are reduced by a cold mirror (heat absorbing filter) so as not to be over 60°C. higher than the temperature of the printed circuit substrate. Such a circuit substrate 1 is set on an automatic parts-loading machine, and the chip-type electronic parts 4 are serially loaded on the gelated adhesive 3 and adequately pressed by a mounted head for adhering the parts on the substrate as shown in FIG. 4(b).

* * *

Hereupon, the adhesive 3 is hardened by heating in the solder reflow process at the same time.

Emphasis added. It is the applicants' position, however, that notwithstanding the fact that Maeda does not teach the simultaneous or concurrent heating and aligning of chips or terminals, the applicants' claimed step of aligning the semiconductor chips during the heating of the adhesive on the substrate at a half-thermosetting temperature is distinguishable over the teaching of the process in Maeda for pressing the electronic parts on the substrate when a "gelated

adhesive 3" has been achieved. That is, two types of fixing are performed in the applicants' claimed method, the first fixing requiring the half-thermosetting temperature and the second fixing at the thermosetting temperature.

It is respectfully submitted that no such two types of fixing are taught in Maeda. As such, the half-thermosetting temperature required for the alignment of the semiconductor chips in the applicants' claimed fabrication method is distinguishable over the mere formation of a "gelated adhesive 3" required for the mere pressing of electronic parts in Maeda.

In view of the above, the applicants have highlighted the above-discussed features of the applicants' claimed fabrication method by further amending claim 1 in the following manner:

wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

In this manner, the applicants further highlight the existence of two sets of fixing in the claimed method, which would add to the importance of having a so-called "tentative fixing"⁵ at the first pressure (different from a subsequent fixing at the second pressure).⁶

⁵ See, lines 15 and 16, page 9 of the applicants' specification.

⁶ That is, as stated in lines 16 - 18, page 11 of the applicants' specification:

the first fixing for the precise alignment is performed in a different process from the pressing and heating.

Also, the fact that the second pressure is greater than the first pressure is supported in lines 4 and 5, page 10 of the applicants' specification. Also, please see the subsequent lines 6 - 13, page 10 of the applicants' specification regarding the advantages or benefits derived from such proposed claim limitations.

It is thus submitted that a person of ordinary skill in the art would not have combined teachings of the cited prior art references in the manner suggested.⁷ Additionally, even if, arguendo, such teachings of the cited prior art can be combined in the manner suggested, such combined teachings would still fall far short in fully meeting the applicants' claimed invention, as now recited in claim 1 (as amended herein). Thus, a person of ordinary skill in the art would not have found the claimed invention, as now set forth in claim 1 (as amended herein) obvious under 35 USC §103 based on the cited prior art references, singly or in combination.

⁷ It is a basic tenet of U.S. patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO Board of Patent Appeals and Interferences in Ex parte Clapp, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the elements of appellants' claimed invention, the prior art itself must actually suggest that the elements be combined in a similar manner as the claimed invention. See, e.g., Panduit Corporation v. Dennison Manufacturing Co., 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), vacated on other grounds, 229 USPQ 478 (U.S. Sup. Ct. 1985).

There is nothing in the prior art to suggest that the elements of the claimed invention present in the cited prior art references can actually be combined to produce applicants' invention embodied in the claims. In fact, the existence in the prior art of all the elements of the claimed invention has not even been established and, thus, the first step in meeting fully the Panduit requirements has not even been reached.

Furthermore, claims 2 - 8 depend on claim 1, and further limit the scope of claim 1. Thus, at least for the reasons set forth above with respect to claim 1, claims 2 - 8 should now be similarly allowable.

In view of the above, the withdrawal of the outstanding rejection under 35 USC §103 based on the applicants' discussion of the prior art⁸ in view of Maeda (U.S. Patent No. 4,880,486), Fujimoto (U.S. Patent No. 5,115,545), and DiStefano (U.S. Patent No. 5,548,091) is in order, and is therefore respectfully solicited.

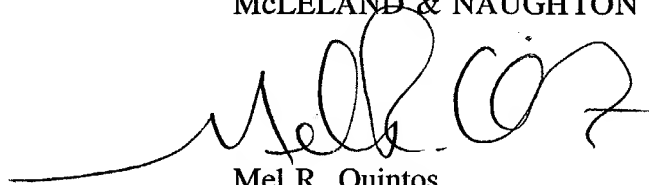
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

⁸ Again, see, line 23, page 1 through line 22, page 2 of the applicants' specification, and as illustrated in the applicants' Figures 1A through 1E.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON

A handwritten signature in black ink, appearing to read 'Mel R. Quintos', is written over the firm name.

Mel R. Quintos
Attorney for Applicants
Reg. No. 31,898

Atty. Docket No. 950107

Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 659-2930

MRQ:ipc
Enclosure: Petition for Extension of Time